

Fig. 1

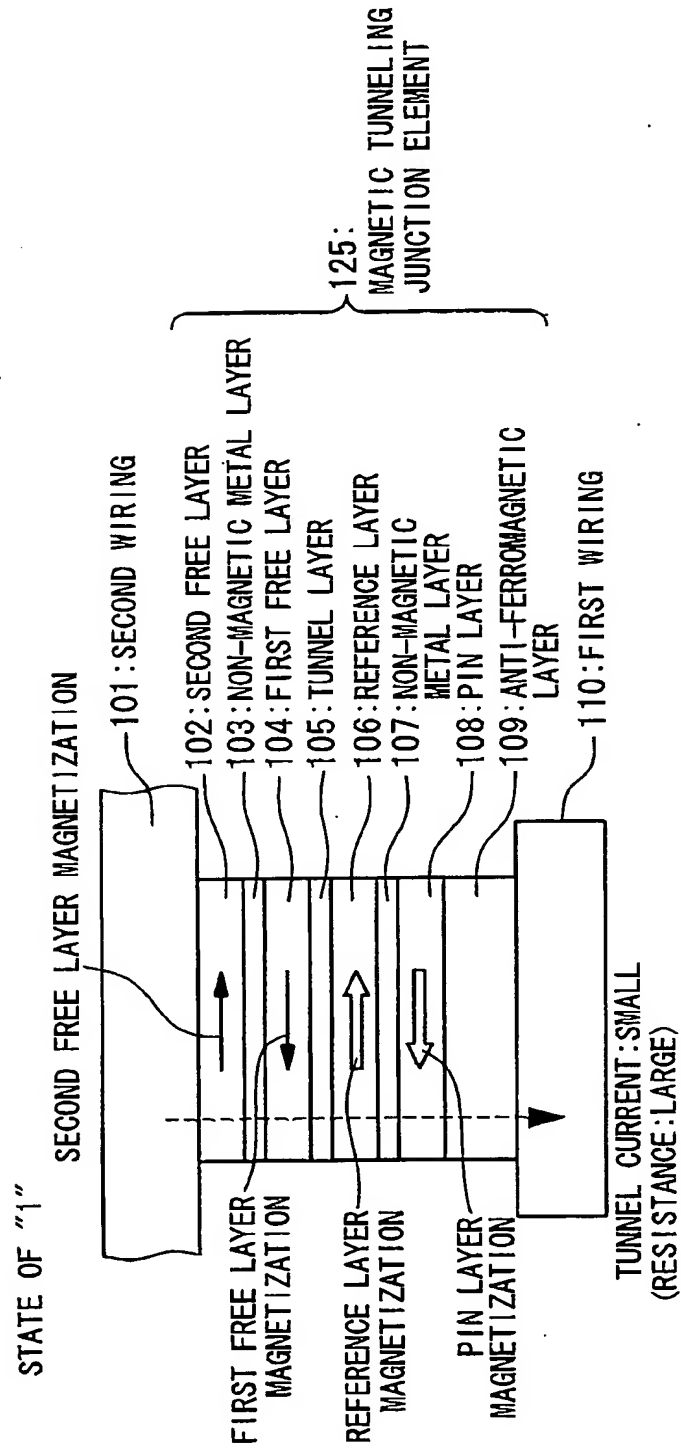


Fig. 2

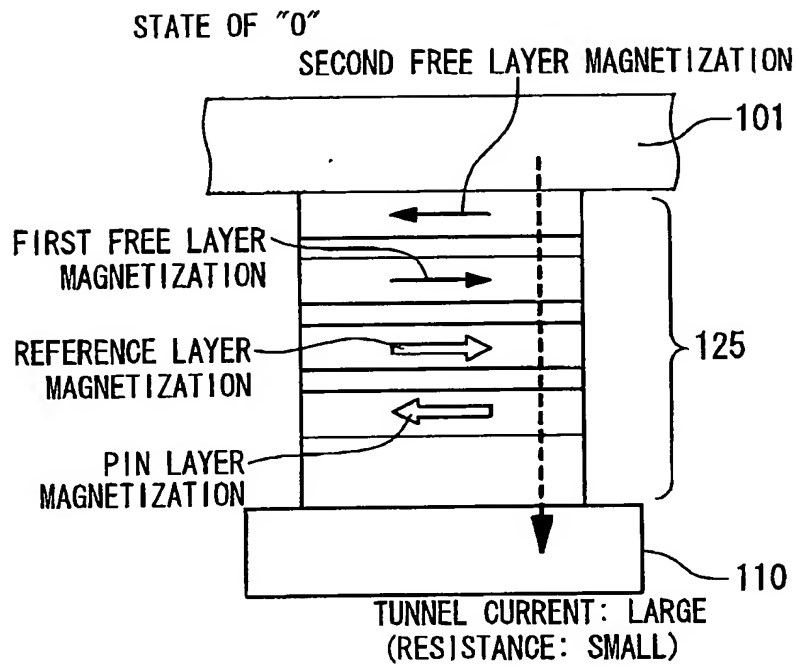


Fig. 3

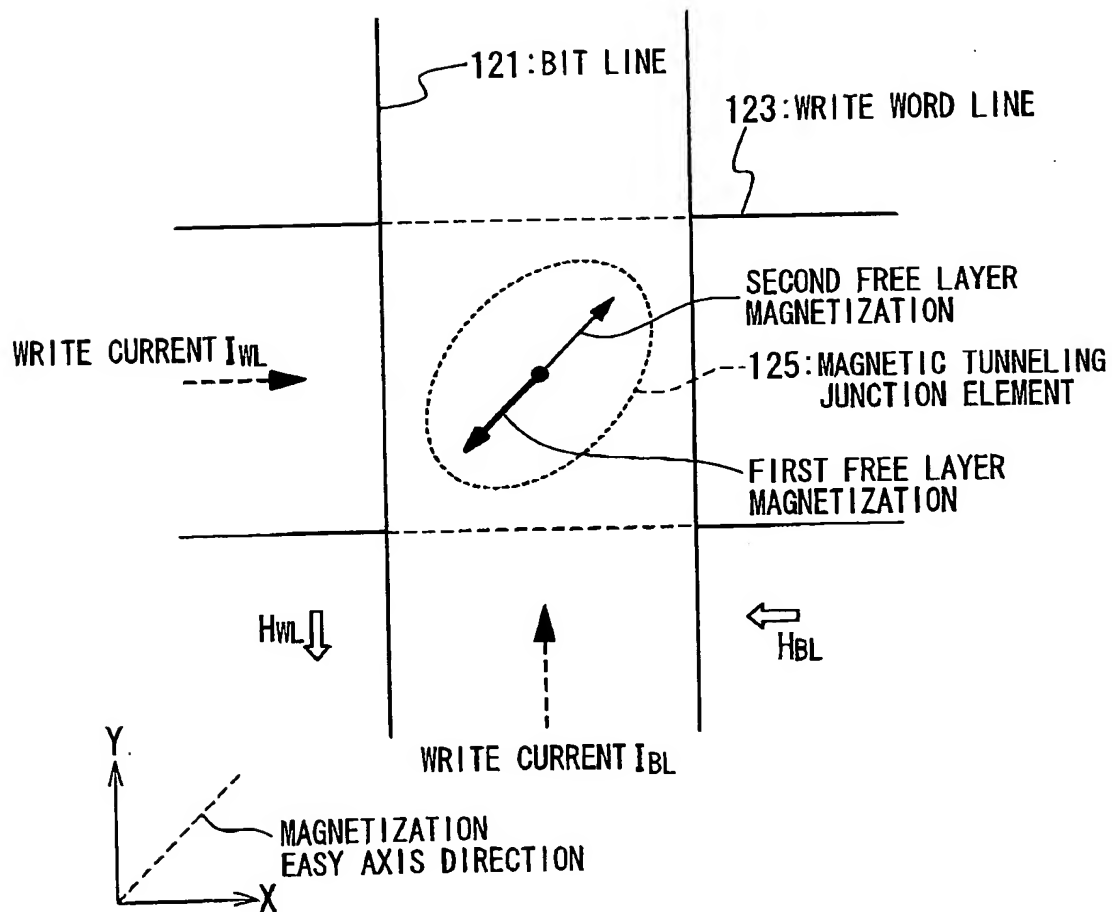


Fig. 4

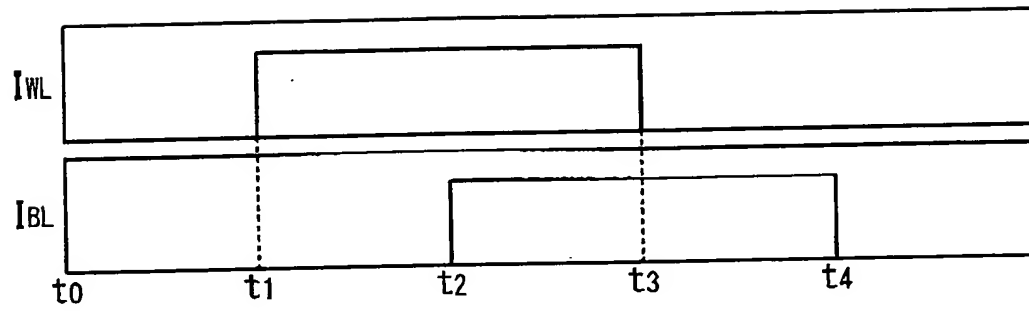


Fig. 5

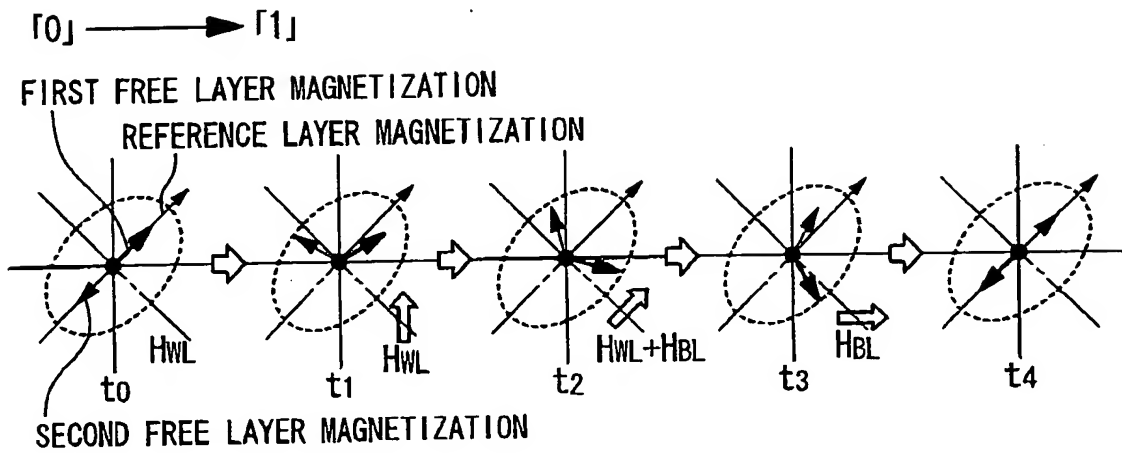


Fig. 6

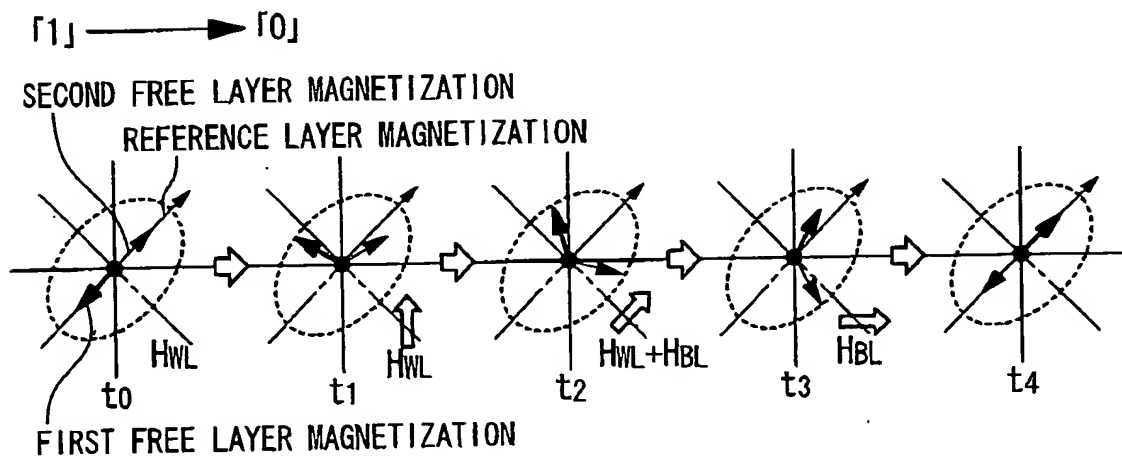
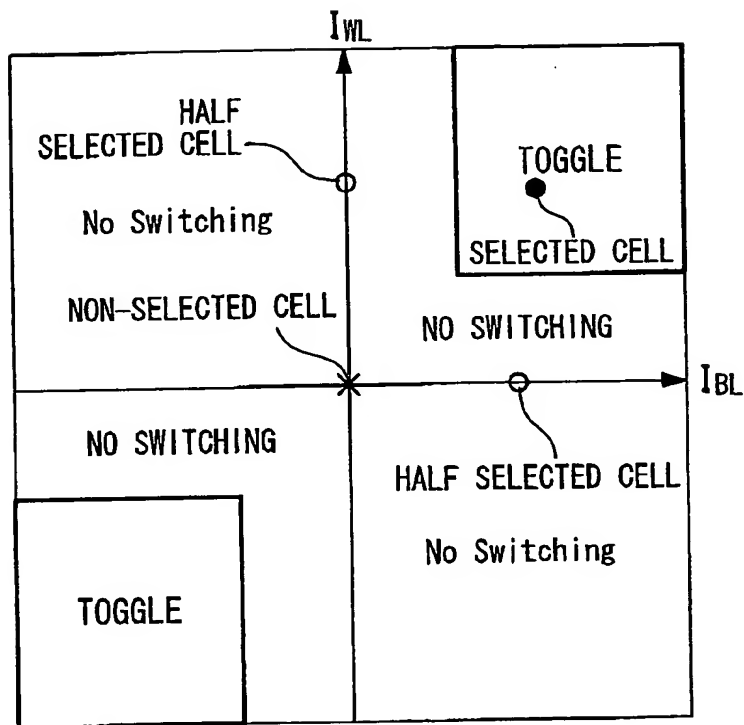
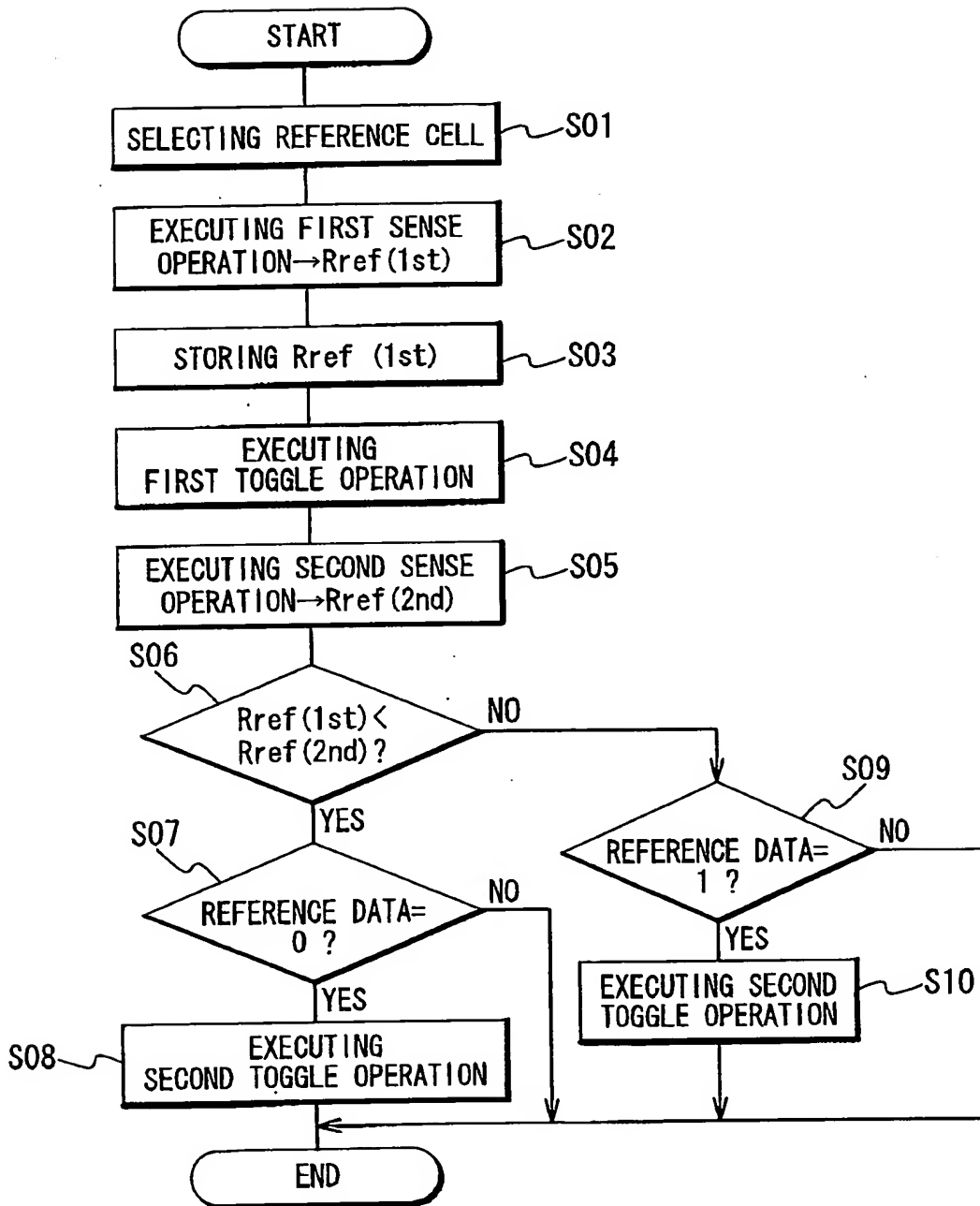


Fig. 7



The diagram illustrates a memory array architecture. At the top, a **Y TERMINATION CIRCUIT** (7) is connected to the array. The array itself consists of a grid of **11: USER AREA REFERENCE CELL** (11), **12: REFERENCE CELL COLUMN** (12), and **11: USER AREA** (11). The array is divided into columns by **23: WRITE WORD LINES** (23) and rows by **24: READ-OUT WORD LINES** (24). The array is terminated by **8: X ADDRESS** (8) and **9: X TERMINATION CIRCUIT** (9). The array is also connected to **14: MEMORY CELL** (14) and **14r: MEMORY CELL** (14r). The array is connected to **25: WRITE CURRENT  $I_{WL}$**  (25) and **25r: WRITE CURRENT  $I_{WL}$**  (25r). The array is connected to **26: READ-OUT CURRENT  $I_R$**  (26) and **26r: READ-OUT CURRENT  $I_R$**  (26r). The array is connected to **21: BIT LINES** (21) and **21r: REFERENCE BIT LINE** (21r). The array is connected to **29** and **29r**. The array is connected to **28: MAIN REFERENCE BIT LINE** (28). The array is connected to **2: FIRST SENSE AMPLIFIER** (2) and **3: SECOND SENSE AMPLIFIER** (3). The array is connected to **1: CONTROLLER** (1). The array is connected to **4: Y ADDRESS** (4) and **5: X ADDRESS** (5). The array is connected to **6: Y DECODER** (6) and **7: X DECODER** (7). The array is connected to **10: FIRST WRITE CURRENT SOURCE** (10) and **11: SECOND WRITE CURRENT SOURCE** (11). The array is connected to **12: RESISTANCE-VOLTAGE CONVERTER** (12) and **13: STORAGE UNIT** (13). The array is connected to **14: DETERMINATION UNIT** (14). The array is connected to **15: Y TERMINATION CIRCUIT** (15) and **16: X TERMINATION CIRCUIT** (16). The array is connected to **17: Y ADDRESS** (17) and **18: X ADDRESS** (18). The array is connected to **19: Y DECODER** (19) and **20: X DECODER** (20). The array is connected to **21: FIRST WRITE CURRENT SOURCE** (21) and **22: SECOND WRITE CURRENT SOURCE** (22). The array is connected to **23: RESISTANCE-VOLTAGE CONVERTER** (23) and **24: STORAGE UNIT** (24). The array is connected to **25: DETERMINATION UNIT** (25). The array is connected to **26: Y TERMINATION CIRCUIT** (26) and **27: X TERMINATION CIRCUIT** (27). The array is connected to **28: Y ADDRESS** (28) and **29: X ADDRESS** (29). The array is connected to **30: Y DECODER** (30) and **31: X DECODER** (31). The array is connected to **32: FIRST WRITE CURRENT SOURCE** (32) and **33: SECOND WRITE CURRENT SOURCE** (33). The array is connected to **34: RESISTANCE-VOLTAGE CONVERTER** (34) and **35: STORAGE UNIT** (35). The array is connected to **36: DETERMINATION UNIT** (36). The array is connected to **37: Y TERMINATION CIRCUIT** (37) and **38: X TERMINATION CIRCUIT** (38). The array is connected to **39: Y ADDRESS** (39) and **40: X ADDRESS** (40). The array is connected to **41: Y DECODER** (41) and **42: X DECODER** (42). The array is connected to **43: FIRST WRITE CURRENT SOURCE** (43) and **44: SECOND WRITE CURRENT SOURCE** (44). The array is connected to **45: RESISTANCE-VOLTAGE CONVERTER** (45) and **46: STORAGE UNIT** (46). The array is connected to **47: DETERMINATION UNIT** (47). The array is connected to **48: Y TERMINATION CIRCUIT** (48) and **49: X TERMINATION CIRCUIT** (49). The array is connected to **50: Y ADDRESS** (50) and **51: X ADDRESS** (51). The array is connected to **52: Y DECODER** (52) and **53: X DECODER** (53). The array is connected to **54: FIRST WRITE CURRENT SOURCE** (54) and **55: SECOND WRITE CURRENT SOURCE** (55). The array is connected to **56: RESISTANCE-VOLTAGE CONVERTER** (56) and **57: STORAGE UNIT** (57). The array is connected to **58: DETERMINATION UNIT** (58). The array is connected to **59: Y TERMINATION CIRCUIT** (59) and **60: X TERMINATION CIRCUIT** (60). The array is connected to **61: Y ADDRESS** (61) and **62: X ADDRESS** (62). The array is connected to **63: Y DECODER** (63) and **64: X DECODER** (64). The array is connected to **65: FIRST WRITE CURRENT SOURCE** (65) and **66: SECOND WRITE CURRENT SOURCE** (66). The array is connected to **67: RESISTANCE-VOLTAGE CONVERTER** (67) and **68: STORAGE UNIT** (68). The array is connected to **69: DETERMINATION UNIT** (69). The array is connected to **70: Y TERMINATION CIRCUIT** (70) and **71: X TERMINATION CIRCUIT** (71). The array is connected to **72: Y ADDRESS** (72) and **73: X ADDRESS** (73). The array is connected to **74: Y DECODER** (74) and **75: X DECODER** (75). The array is connected to **76: FIRST WRITE CURRENT SOURCE** (76) and **77: SECOND WRITE CURRENT SOURCE** (77). The array is connected to **78: RESISTANCE-VOLTAGE CONVERTER** (78) and **79: STORAGE UNIT** (79). The array is connected to **80: DETERMINATION UNIT** (80). The array is connected to **81: Y TERMINATION CIRCUIT** (81) and **82: X TERMINATION CIRCUIT** (82). The array is connected to **83: Y ADDRESS** (83) and **84: X ADDRESS** (84). The array is connected to **85: Y DECODER** (85) and **86: X DECODER** (86). The array is connected to **87: FIRST WRITE CURRENT SOURCE** (87) and **88: SECOND WRITE CURRENT SOURCE** (88). The array is connected to **89: RESISTANCE-VOLTAGE CONVERTER** (89) and **90: STORAGE UNIT** (90). The array is connected to **91: DETERMINATION UNIT** (91). The array is connected to **92: Y TERMINATION CIRCUIT** (92) and **93: X TERMINATION CIRCUIT** (93). The array is connected to **94: Y ADDRESS** (94) and **95: X ADDRESS** (95). The array is connected to **96: Y DECODER** (96) and **97: X DECODER** (97). The array is connected to **98: FIRST WRITE CURRENT SOURCE** (98) and **99: SECOND WRITE CURRENT SOURCE** (99). The array is connected to **100: RESISTANCE-VOLTAGE CONVERTER** (100) and **101: STORAGE UNIT** (101). The array is connected to **102: DETERMINATION UNIT** (102). The array is connected to **103: Y TERMINATION CIRCUIT** (103) and **104: X TERMINATION CIRCUIT** (104). The array is connected to **105: Y ADDRESS** (105) and **106: X ADDRESS** (106). The array is connected to **107: Y DECODER** (107) and **108: X DECODER** (108). The array is connected to **109: FIRST WRITE CURRENT SOURCE** (109) and **110: SECOND WRITE CURRENT SOURCE** (110). The array is connected to **111: RESISTANCE-VOLTAGE CONVERTER** (111) and **112: STORAGE UNIT** (112). The array is connected to **113: DETERMINATION UNIT** (113). The array is connected to **114: Y TERMINATION CIRCUIT** (114) and **115: X TERMINATION CIRCUIT** (115). The array is connected to **116: Y ADDRESS** (116) and **117: X ADDRESS** (117). The array is connected to **118: Y DECODER** (118) and **119: X DECODER** (119). The array is connected to **120: FIRST WRITE CURRENT SOURCE** (120) and **121: SECOND WRITE CURRENT SOURCE** (121). The array is connected to **122: RESISTANCE-VOLTAGE CONVERTER** (122) and **123: STORAGE UNIT** (123). The array is connected to **124: DETERMINATION UNIT** (124). The array is connected to **125: Y TERMINATION CIRCUIT** (125) and **126: X TERMINATION CIRCUIT** (126). The array is connected to **127: Y ADDRESS** (127) and **128: X ADDRESS** (128). The array is connected to **129: Y DECODER** (129) and **130: X DECODER** (130). The array is connected to **131: FIRST WRITE CURRENT SOURCE** (131) and **132: SECOND WRITE CURRENT SOURCE** (132). The array is connected to **133: RESISTANCE-VOLTAGE CONVERTER** (133) and **134: STORAGE UNIT** (134). The array is connected to **135: DETERMINATION UNIT** (135). The array is connected to **136: Y TERMINATION CIRCUIT** (136) and **137: X TERMINATION CIRCUIT** (137). The array is connected to **138: Y ADDRESS** (138) and **139: X ADDRESS** (139). The array is connected to **140: Y DECODER** (140) and **141: X DECODER** (141). The array is connected to **142: FIRST WRITE CURRENT SOURCE** (142) and **143: SECOND WRITE CURRENT SOURCE** (143). The array is connected to **144: RESISTANCE-VOLTAGE CONVERTER** (144) and **145: STORAGE UNIT** (145). The array is connected to **146: DETERMINATION UNIT** (146). The array is connected to **147: Y TERMINATION CIRCUIT** (147) and **148: X TERMINATION CIRCUIT** (148). The array is connected to **149: Y ADDRESS** (149) and **150: X ADDRESS** (150). The array is connected to **151: Y DECODER** (151) and **152: X DECODER** (152). The array is connected to **153: FIRST WRITE CURRENT SOURCE** (153) and **154: SECOND WRITE CURRENT SOURCE** (154). The array is connected to **155: RESISTANCE-VOLTAGE CONVERTER** (155) and **156: STORAGE UNIT** (156). The array is connected to **157: DETERMINATION UNIT** (157). The array is connected to **158: Y TERMINATION CIRCUIT** (158) and **159: X TERMINATION CIRCUIT** (159). The array is connected to **160: Y ADDRESS** (160) and **161: X ADDRESS** (161). The array is connected to **162: Y DECODER** (162) and **163: X DECODER** (163). The array is connected to **164: FIRST WRITE CURRENT SOURCE** (164) and **165: SECOND WRITE CURRENT SOURCE** (165). The array is connected to **166: RESISTANCE-VOLTAGE CONVERTER** (166) and **167: STORAGE UNIT** (167). The array is connected to **168: DETERMINATION UNIT** (168). The array is connected to **169: Y TERMINATION CIRCUIT** (169) and **170: X TERMINATION CIRCUIT** (170). The array is connected to **171: Y ADDRESS** (171) and **172: X ADDRESS** (172). The array is connected to **173: Y DECODER** (173) and **174: X DECODER** (174). The array is connected to **175: FIRST WRITE**

Fig. 9





The diagram illustrates a sense amplifier circuit for a memory array. The circuit is organized into several functional blocks:

- 3: SECOND SENSE AMPLIFIER** (Overall block):
  - 31: RESISTANCE-VOLTAGE CONVERTER**: Consists of a resistor  $R_{ref}$  and a load capacitor  $C_c$  connected to a reference current source  $I_r$ .
  - 32: STORAGE UNIT**: A capacitor  $C_c$  that stores the voltage  $V_{ref}$  across  $R_{ref}$ .
  - 33: DETERMINATION UNIT**: A differential amplifier stage consisting of a first switch unit (43) and a second switch unit (45).
- 28: MAIN REFERENCE BIT LINE**: A horizontal line that carries the reference current  $I_r$  and the reference voltage  $V_{ref}$ .
- 21r: REFERENCE BIT LINE**: A vertical line that carries the reference current  $I_r$  and the reference voltage  $V_{ref}$ .
- 24: READ-OUT WORD LINES**: A set of horizontal lines that connect the reference bit lines to the reference cells.
- 14r: REFERENCE CELL**: A cell that provides a reference voltage  $V_{ref}$  to the reference bit line.
- 10: CELL ARRAY**: The overall array of cells.
- 41**: A transistor that provides a reference current  $I_r$  to the reference bit line.
- 42: LOAD CAPACITOR**: A capacitor  $C_c$  that is connected to the reference bit line.
- 43: FIRST SWITCH UNIT**: A switch controlled by  $\phi_1$  that connects the reference bit line to the first input of the differential amplifier.
- 44**: A transistor that provides a reference current  $I_r$  to the reference bit line.
- 45: SECOND SWITCH UNIT**: A switch controlled by  $\phi_2$  that connects the reference bit line to the second input of the differential amplifier.
- 46**: A differential amplifier that compares the voltages at its two inputs and produces a differential output  $V_o$ .
- 47: LATCH CIRCUIT**: A latch circuit that latches the output of the differential amplifier.
- 48: EXCLUSIVE LOGICAL SUM GATE**: A gate that produces the final output  $DOUT$  based on the latched signal and the  $TG2EN$  signal.

Fig. 11

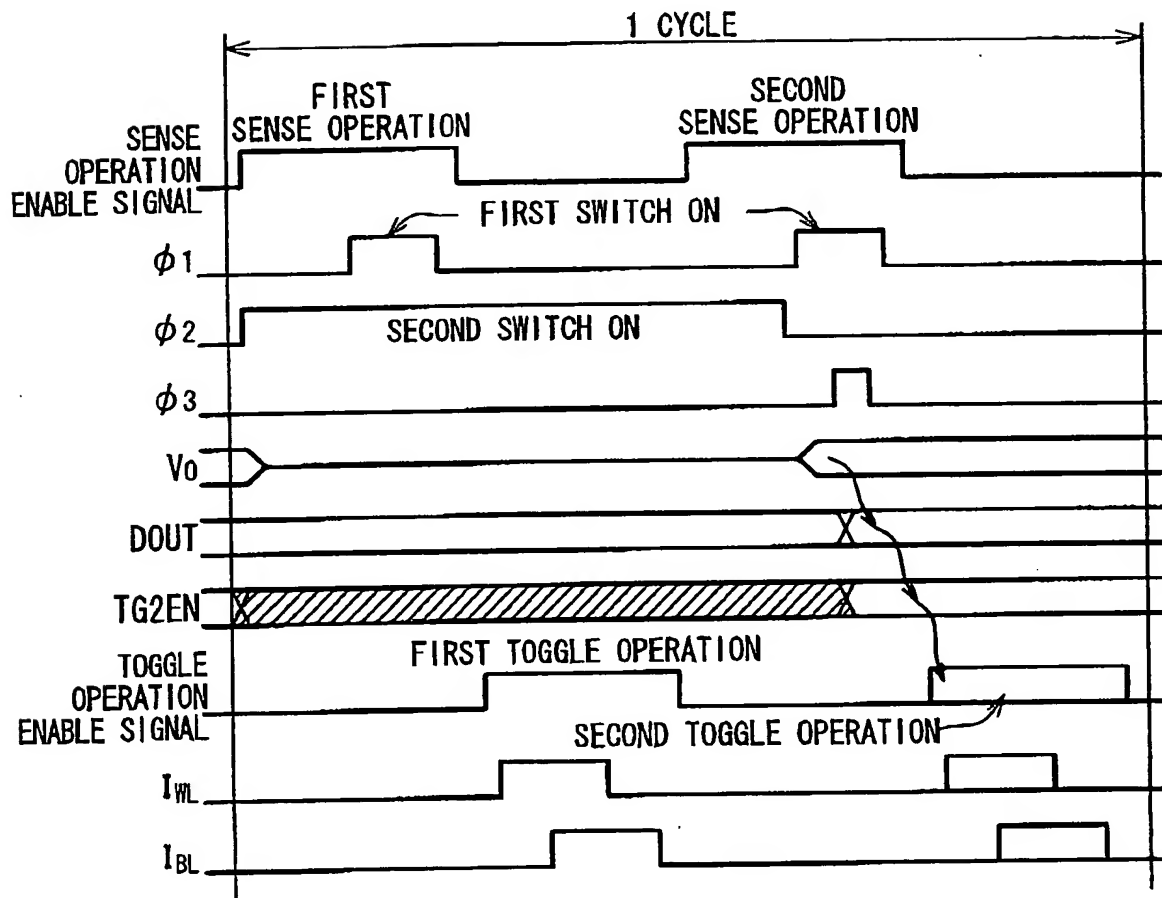
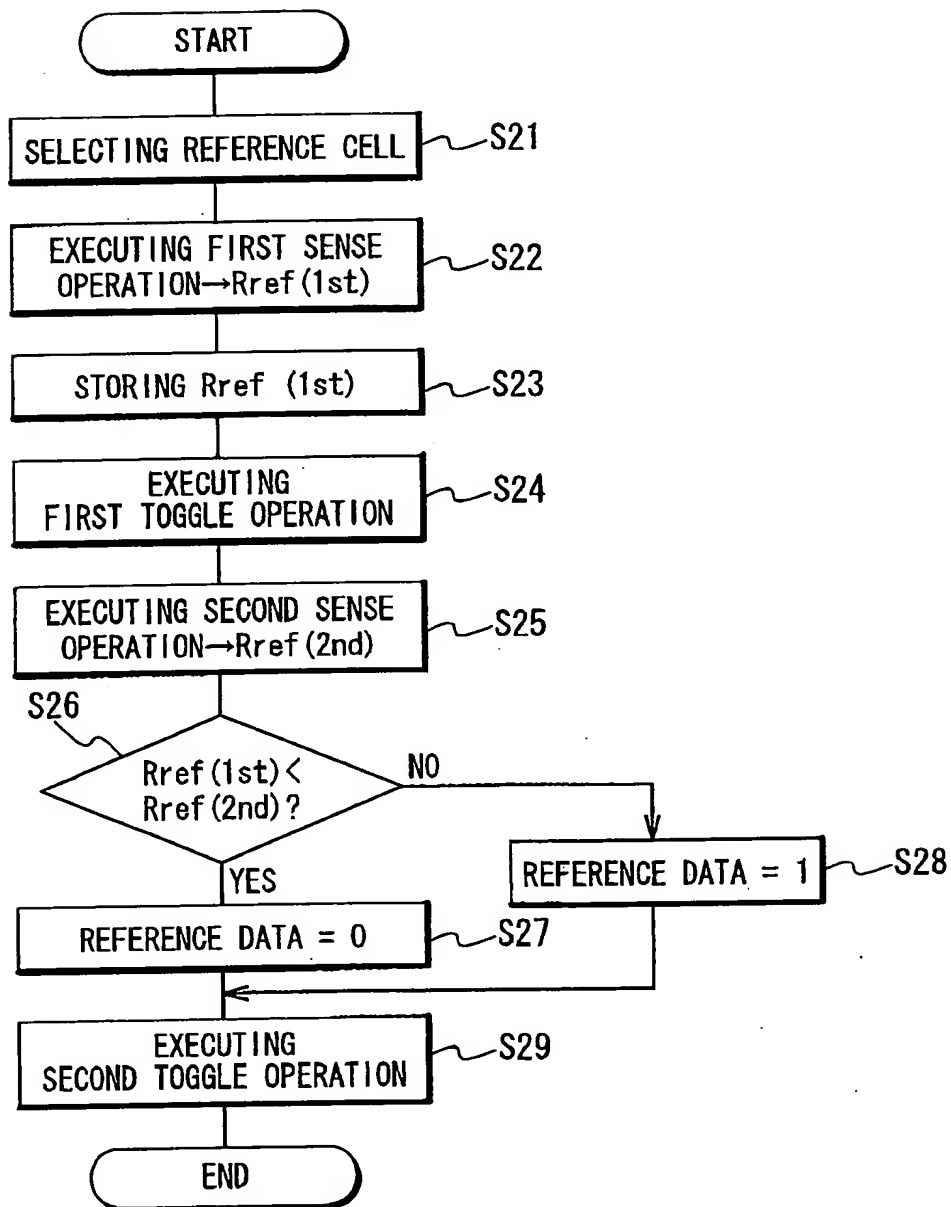




Fig. 14



[illegible]

Fig. 16

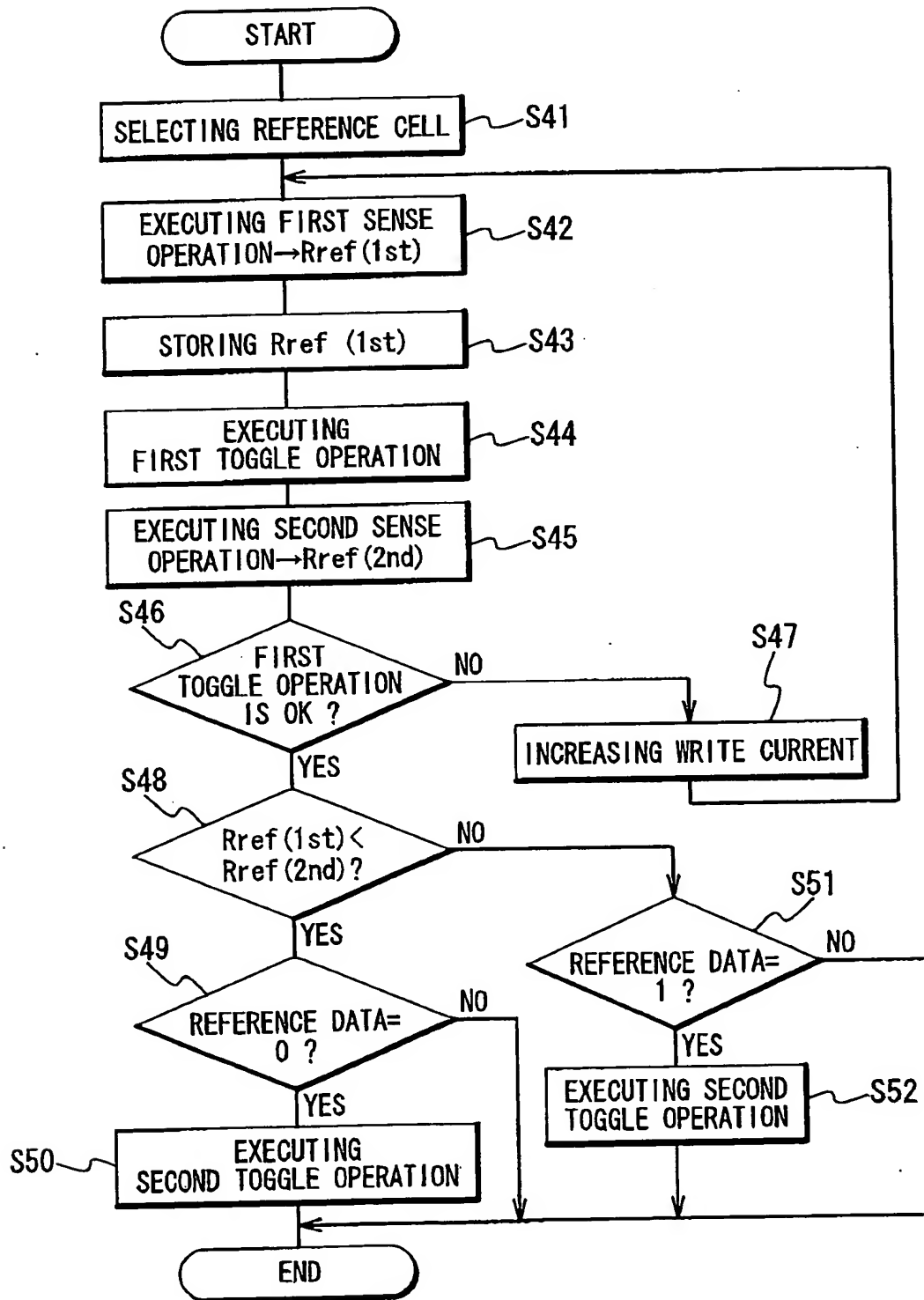




Fig. 18

ID	REFERENCE INFORMATION	Q1	Q2	DOUT	TG2EN	TGERR
1	0	0	0	0	1	0
2	0	0	1	X	0	1
3	0	1	0	X	0	1
4	0	1	1	1	0	0
5	1	0	0	0	0	0
6	1	0	1	X	0	1
7	1	1	0	X	0	1
8	1	1	1	1	1	0



Fig. 19

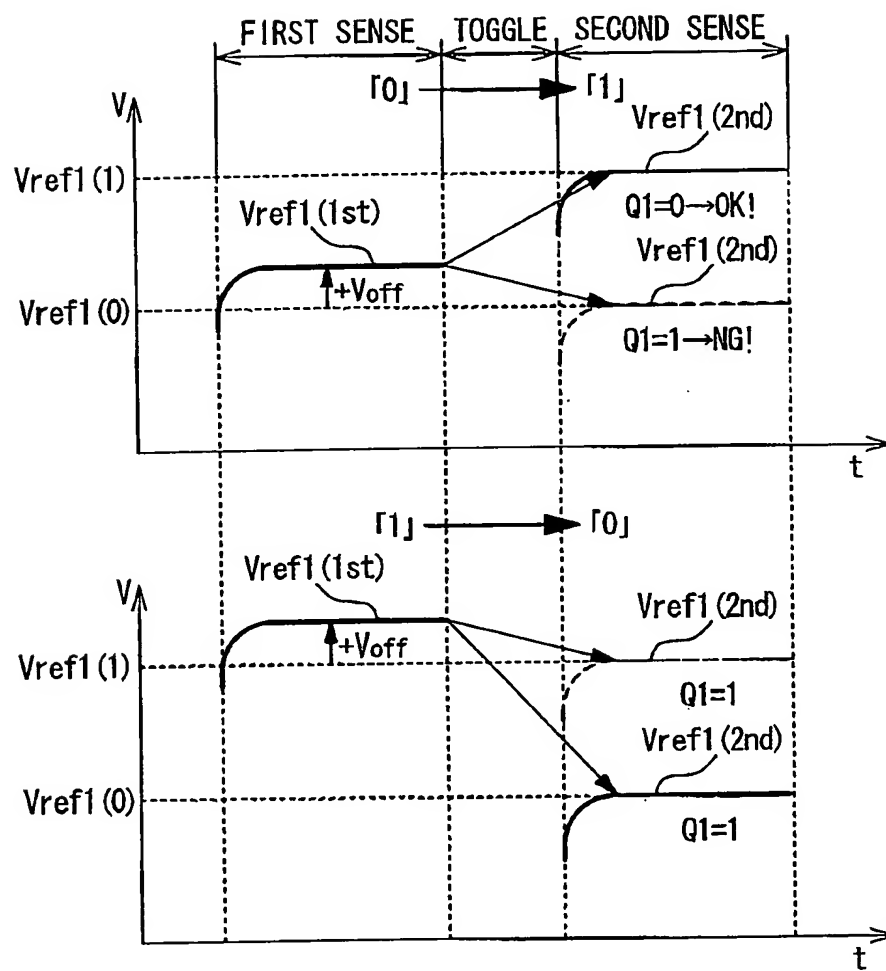


Fig. 20

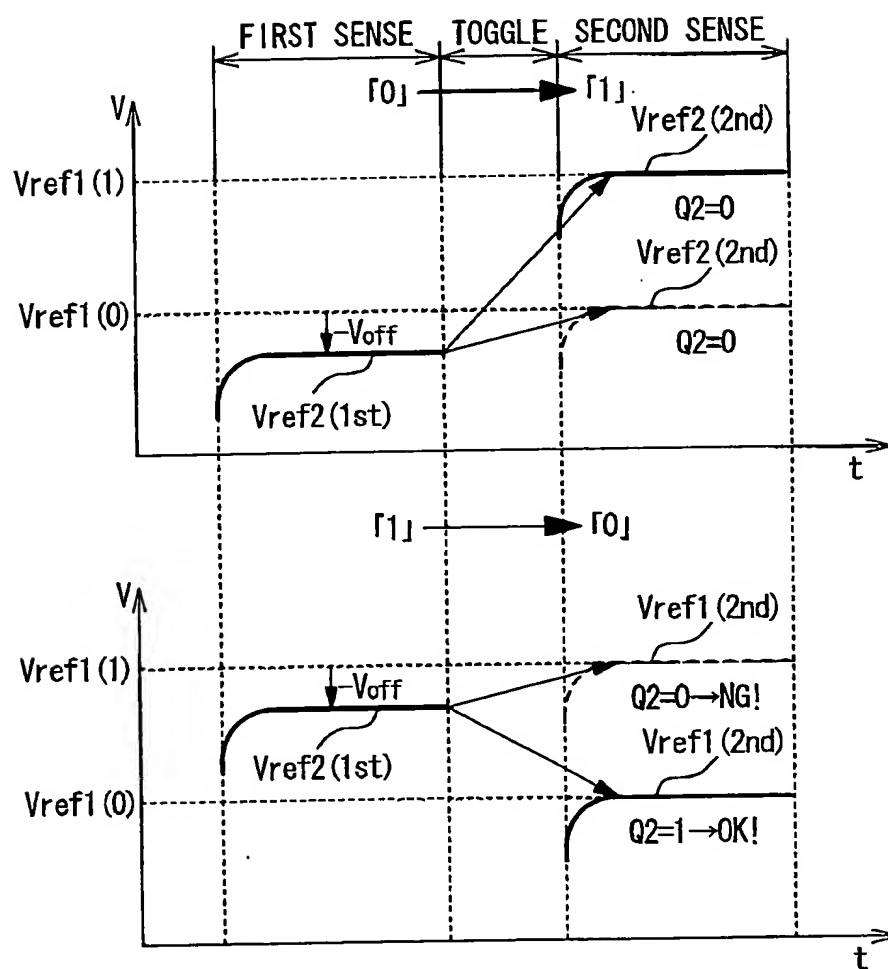


Fig. 21

